Case Docket No. PHF 98,601

THE COMMISSIONER OF PATENTS AND TRADEMARKS, Washington, D.C. 20231

Enclosed for filing is the patent application of Inventor:
PIERRE BAUDET and PETER FRIJLINK

SEMICONDUCTOR DEVICE WITH INTEGRATED CIRCUIT ELEMENTS OF GROUP III-V COMPRISING MEANS FOR PREVENTING POLLUTION BY HYDROGEN

ENCLOSED ARE:

[X] Appointment of Associates;
[X] Information Disclosure Statement, Form PTO-1449 and copies of documents listed therein;
[X] Preliminary Amendment;
[X] Specification (9 Pages of Specification, Claims, & Abstract);
[X] Declaration and Power of Attorney:
(1 Page of a [ ]fully executed [X]unsigned Declaration);
[X] Drawing (2 sheets of [X]informal [ ]formal sheets);
[X] Certified copy of FRENCH application Serial 9812497;
[X] Authorization Pursuant to 37 CFR §1.136(a)(3)
[ ] Other: ;
[ ] Assignment to

FEE COMPUTATION

CLAIMS AS FILED				
FOR	NUMBER FILED	NUMBER EXTRA	RATE	BASIC FEE - $760.00
Total Claims	10 - 20 =		X $18 =	0.00
Independent Claims	1 - 3 =		X $78 =	0.00
Multiple Dependent Claims, if any			$260 =	0.00
TOTAL FILING FEE			=	$760.00

Please charge Deposit Account No. 14-1270 in the amount of the total filing fee indicated above, plus any deficiencies. The Commissioner is also hereby authorized to charge any other fees which may be required, except the issue fee, or credit any overpayment to Account No. 14-1270.

[ ]Amend the specification by inserting before the first line as a centered heading --Cross Reference to Related Applications--; and insert below that as a new paragraph --This is a continuation-in-part of application Serial No. , filed , which is herein incorporated by reference--.

CERTIFICATE OF EXPRESS MAILING

Express Mail Mailing Label No. EL 458 217 735 US
Date of Deposit October 5, 1999
I hereby certify that this paper and/or fee is being deposited with the United States Postal Service "Express Mail Post Office to Addressee" service under 37 C.F.R. 1.10 on the date indicated above and is addressed to the Commissioner of Patents and Trademarks, Washington, D.C. 20231.

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Typed Name **Signature**

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of | Atty. Docket

PIERRE BAUDET ET AL | PHF 98,601

Serial No.

Filed: CONCURRENTLY

SEMICONDUCTOR DEVICE WITH INTEGRATED CIRCUIT ELEMENTS OF GROUP III-V COMPRISING MEANS FOR PREVENTING POLLUTION BY HYDROGEN

Honorable Commissioner of Patents and Trademarks
Washington, D.C. 20231

PRELIMINARY AMENDMENT

Sir:

Prior to calculation of the filing fee and examination, please amend the above-identified application as follows:

IN THE TITLE

Please change the title to all capitals and delete "." (period).

IN THE CLAIMS

Page 7, before line 1, replace "CLAIMS" with

--WHAT IS CLAIMED IS:--

Claim 4, line 1, delete "or as claimed in one of the claims 2 and 3,".

Claim 5, line 1, change "one of the claims 1 to 4" to --claim 1--.

Claim 6, line 1, change "any one of the claims 1 to 5" to --claim 1--.

Claim 7, line 1, change "any one of the claims 1 to 5" to --claim 1--.

Claim 8, line 1, change "any one of the claims 1 to 7" to --claim 1--.

Claim 9, line 1, change "any one of the claims 1 to 8" to --claim 1--.

Claim 10, line 1, change "any one of the claims 1 to 8" to --claim 1--.

IN THE ABSTRACT

Before line 1, delete in its entirety and substitute the following as a centered heading:

--ABSTRACT OF THE DISCLOSURE--;

line 8, continue on line 7;

delete lines 11-12 in their entirety.

REMARKS

The Abstract has been amended to add headings in accordance with MPEP Section 601. The claims have been amended in order to reformat the claims to delete all multiple dependencies prior to calculation of the filing fee and place the instant application in standard U.S. format.

Entry of this amendment prior to calculating the filing fee is respectfully requested.

Respectfully submitted,

By _____
Steven R. Biren, Reg.26,531
Attorney
(914) 333-9630

Semiconductor device with integrated circuit elements of group III-V comprising means for preventing pollution by hydrogen.

FIELD OF THE INVENTION

The invention relates to a semiconductor device comprising integrated circuit elements realized in a stack of layers on a substrate and comprising means for preventing pollution of the circuit elements and of the substrate by hydrogen originating from their environment.

The invention finds its application in the semiconductor manufacturing industry, including the manufacture of integrated circuits which are incorporated in hermetically sealed modules such as transmission modules used in the field of telecommunications.

BACKGROUND OF THE INVENTION

A semiconductor device comprising means for preventing the pollution of circuit elements by hydrogen is known from patent application JP no. 64-207266 of 10.08.1989 published 27.03.1991 (FUJITSU LTD.; TAKAYUKI OBA). This patent application describes means for preventing the hydrogen from diffusing into the semiconductor substrate, thus improving the reliability of a semiconductor device. These means consist of a layer which absorbs the hydrogen contained in insulating layers.

The use of these means involves the realization of a composite film comprising a metal layer made of a metal which absorbs the hydrogen, forming a hydride, arranged in sandwich fashion between two insulating layers of silicon nitride (SiN). This composite film is deposited on the upper surface of a semiconductor device which comprises a substrate and a circuit element formed on said substrate. The insulating layer, which contains nitrogen (N), such as the silicon nitride (SiN) layer, contains much hydrogen. The metal layer which is sandwiched between the insulating layers absorbs this hydrogen. A suitable metal for absorbing the hydrogen is palladium. For example, the composite film is formed by the metal layer of palladium sandwiched between two layers of silicon nitride. The result of this is that the hydrogen present within a protective insulating layer formed at the upper surface of the semiconductor device and the hydrogen present within an intermediate insulating layer can be captured by the sandwiched metal layer. The diffusion of the hydrogen into the substrate is

thus suppressed and the generation of hot electrons in the substrate can be reduced to a minimum.

SUMMARY OF THE INVENTION

It is an object of the invention to provide means for eliminating the hydrogen originating more in particular from the environment of an integrated semiconductor device when this semiconductor device is protected by a housing. It is known to those skilled in the art that the metal parts of protective housings of "chips" or integrated semiconductor devices are subject to aging, during which they evolve especially hydrogen. If the semiconductor device is realized on a substrate of a material from group III-V, for example gallium arsenide, the hydrogen will react with the substrate material and act as a neutralizer of charges, either at the surface or inside the material itself. If the semiconductor device comprises a stack of epitaxial layers and one of these materials is from the group III-V, the hydrogen will act as a charge neutralizer at the interfaces of the layers or inside the layers. The diffusion of hydrogen thus has a major detrimental effect on the surface charges, the interface charges, and on the doping profiles of the substrate and the layers.

This phenomenon is generally referred to as hydrogen poisoning. Its effect may become apparent at temperatures of the order of 100 °C and higher. It should be borne in mind that the operational standards in the field of integrated circuits may demand that the circuits operate at temperatures of up to 125 °C, or even up to 200 or 300 °C without any deterioration in performance, depending on the envisaged application. In particular, a circuit included in a module which is launched in a telecommunication satellite must be capable of operating at temperatures of the order of 300 °C. It is found that from the moment when a semiconductor device of the type described above is enclosed in a protective housing, this semiconductor device exhibits a deterioration in its performance within a very short time, of the order of a few hundred hours, or even just a few hours, depending on the temperature at which it is made to operate. Experiments have shown that the use of a metal layer made of a hydrogen-absorbing metal sandwiched between two insulating layers so as to form a composite film covering the integrated circuits has a detrimental influence on the integrated circuit because this composite film constitutes a strong parasitic capacitance which downgrades the performance levels of all elements of the integrated circuit even at room temperature. Such a layer realized in accordance with the cited patent application should accordingly be steered clear of altogether.

The cited document teaches that the hydrogen originates from the insulating layers themselves. Experiments have accordingly been carried out for verifying the presence

of this problem and these experiments have shown that the effect produced thereby is negligible. Indeed, it is the hydrogen originating from the environment of the semiconductor device, and in particular from the housing, which has a very important detrimental effect.

According to the invention, this detrimental effect is suppressed by means of a device provided with means as defined in claim 1.

An advantage of the device according to the invention is that the detrimental effect of the hydrogen on the integrated circuit elements is no longer present once this device has been enclosed in a housing. The deterioration in performance of the integrated circuits can no longer be observed in time. It follows from this that the hydrogen contained in the integrated circuit itself is not the major factor of deterioration as taught in the cited patent application. But whatever the cause, the means according to the invention also solve the problem known from the cited patent application.

BRIEF DESCRIPTION OF THE DRAWINGS

The invention will now be explained in more detail below with reference to the annexed diagrammatic Figures, in which:

Fig. 1A is a plan view of a semiconductor device with an example of an integrated circuit element on a substrate provided with a hydrogen getter;

Fig. 1B shows the device of Fig. 1 in cross-section; and

Figs. 2A, 2B, 2C illustrate steps in a process for the manufacture of a hydrogen getter included in an integrated circuit of a semiconductor device.

DESCRIPTION OF PREFERRED EMBODIMENTS

The invention relates to an integrated semiconductor device comprising circuit elements realized in a stack of layers on a substrate made from materials from the chemical group III-V. These groups III-V materials lose their electrical properties in a few hours if present in an environment containing hydrogen and at a temperature higher than room temperature.

The invention provides means integrated with the circuit elements on the substrate for eliminating the hydrogen from the environment.

The expression "hydrogen from the environment" is understood to mean the hydrogen which is enclosed together with the integrated circuit device inside a hermetically sealed protective housing. The hydrogen present in said environment originates essentially from metal elements of the housing, which degasses in the course of time owing to aging or to the temperature which is higher than room temperature.

The expression "temperature higher than room temperature" is understood to mean any temperature, for example, lying between 30 °C and 300 °C which may arise when the device is used in a system launched in a satellite, or used on earth for telecommunication purposes. In general, the operating temperature will be of the order of 100 °C to 250 °C.

Under these conditions, it was found that the hydrogen in question does not originate from parts of the integrated circuits or from insulating layers of the integrated circuit to any appreciable degree, but on the contrary from degassing of metal parts or other parts of the housing, and that this degassing takes place even if the housing had already been degassed before use.

According to the invention, a layer portion of a material which absorbs hydrogen is provided on a region of the surface of the integrated circuit. This layer portion, which may have any shape as desired, is realized in the regions without circuit elements, for example between circuit elements, or alternatively peripheral to the integrated circuits, taking into account manufacturing tolerances which define the distances between the circuit elements.

Palladium (Pd) is a metal which has given the best results as a hydrogen-absorbing material up to the present day. It is by no means impossible, however, that those skilled in the art will find other materials or metals which have equally good properties. In that case, these materials or metals may be used as palladium is here. Titanium (Ti), on its own or in combination with palladium (Pd) is also known to give satisfactory results. Generally, materials comprising palladium or materials comprising titanium, or both, may be favorably used for realizing a hydrogen getter.

Fig. 1A shows an example of an embodiment of a semiconductor device, in plan view, with an integrated circuit element 21 and a pattern 10 of a material which absorbs hydrogen. The integrated circuit element 21 is a field effect transistor with a gate G, a source S, and a drain D. The pattern 10 of the material which absorbs hydrogen is a rectangle. This pattern, however, may have any shape whatsoever so as to be accommodated between the circuit elements.

Fig. 1B shows the same semiconductor device in cross-section taken on the line AA' in Fig. 1A. The semiconductor device comprises a stack of layers 2 to 5 of group III-V material realized on a substrate 1 of gallium arsenide (GaAs). The stack of layers comprises regions 17 for lateral insulation of a circuit element from other circuit elements, and at least one active region 12 for realizing a circuit element which in the example given here is a PHEMT (Pseudomorphic High Electron Mobility Transistor) or pseudomorphic HEMT.

Fig. 2A shows a stack of epitaxial layers realized on a semi-insulating substrate 1 made of GaAs for the realization of a PHEMT, by way of non-limitative example. This stack comprises, starting from the substrate: a buffer layer 2 of undoped GaAs with a thickness of the order of 0.5 to 1 μm; two mutually adjoining layers which form a heterostructure, i.e. having different forbidden bandwidths or gaps, with the layer 3 of InGaAs which is not doped, has the smaller forbidden bandwidth, and has a thickness of the order of 10 to 15 nm, and with the layer 4 of AlGaAs which is n^+ doped and has a thickness of approximately 20 to 50 nm; and then a covering layer 5 of n^+ doped GaAs with a thickness of approximately 20 to 50 nm. The layer 4 forms an etch stop layer with respect to the layer 5.

In a step following the realization of the layers, an ion implantation is carried out in the zones 17 so as to define the active region 12.

In Fig. 2B, a layer 10, for example made of palladium, is now realized so as to form the hydrogen-absorbing pattern in the given shape (for example, a rectangle between two transistors).

In Fig. 2C, the pattern is now protected by a mask M of a material which renders it possible to realize the transistor in region 21 by standard methods known to those skilled in the art and which may be eliminated once the transistor has been completed.

In Fig. 1B, the mask M protecting the pattern 10 has been removed after completion of the transistor 21, and the assembly of the semiconductor device is covered with a protective layer, which may be made of silicon oxide (SiO_2) or silicon nitride (SiN).

Fig. 1B, which corresponds to Fig. 1A, shows that the gate G, the drain D, and the source S are covered by conducting layers CG, CD, and CS, respectively, called contacts of the second level and serving to connect said electrodes G, D, S to other elements of the integrated circuit.

According to the invention, a protective layer 20 covers the entire integrated circuit, but it is very important that it should comprise an opening AP for exposing the upper surface 11 of the layer 10 of hydrogen-absorbing material.

The integrated circuit provided with the layer 10 for absorbing hydrogen does not have the disadvantage that it introduces parasitic capacitance's, as in the device described with reference to the prior art. Once the semiconductor device has been enclosed in its protective housing, it is found that the deteriorations in performance, which manifest themselves before the type of hydrogen getter formed by the layer 10 according to the invention has been applied, do not arise any longer. This appears to prove that the real problem is indeed caused by the presence of hydrogen in the environment of the

semiconductor device and not by the quantity of hydrogen present in the layers of the integrated circuit itself, the latter quantity being certainly negligible.

The manufacture of MMIC transistors or circuit elements realized by means of materials of group III-V often involves the use of palladium for separating aluminum (Al) layers from gold (Au) layers because aluminum and gold are incompatible. The realization of a palladium layer 10 as a hydrogen getter in that case will not necessitate an additional manufacturing step: it is sufficient to reserve the location for the palladium pattern 10 and subsequently to realize this pattern simultaneously with the Al/Au separating layers. The layer 10 is therefore not necessarily formed directly on the substrate. The sole requirement is that its upper surface 11 must be exposed.

Palladium has the characteristic that it absorbs approximately 900 times its own volume of hydrogen, forming a compound Pd_2H. The presence of a layer 10 of palladium of a sufficiently great surface area and thickness accordingly prevents the hydrogen originating from the environment of the circuit from affecting the small quantity of palladium which is involved in the process of manufacturing MMIC transistors made from group III-V materials. In addition, the presence of the layer 10 forming the hydrogen getter prevents the neutralization of charges in the III-V layers or at the interfaces thereof.

The device comprising one or several integrated circuits as described above is encapsulated in a housing. The housing is preferably hermetically closed.

This device may form part of a spatial telecommunication module or system launched in an artificial satellite, or alternatively in a terrestrial telecommunication module or system.

The integrated circuits may form transmission/reception circuits, amplifiers, phase shifters, or any other circuits used in the modules of telecommunication systems. Generally, these circuits operate at high and microwave frequencies and are called MMICs (Monolithic Microwave Integrated Circuits).

CLAIMS:

1. A semiconductor device comprising integrated circuit elements realized in a stack of layers on a substrate and comprising means for preventing pollution of the circuit elements and of the substrate by hydrogen originating from their environment, characterized in that said means are formed by a layer of a material which absorbs hydrogen, referred to as hydrogen getter (10), which forms a pattern which is integrated with the circuit elements and of which an external surface (11) is exposed and in contact with said environment.

2. A device as claimed in claim 1, characterized in that the hydrogen getter layer is formed on the surface of the substrate and in that the circuit elements comprise an upper protective layer which has an opening for exposing the upper surface (11) of said hydrogen getter layer (10).

3. A device as claimed in claim 1, characterized in that the hydrogen getter layer is realized simultaneously with a layer of a same material from which elements of the integrated circuits are formed, and in that the circuit elements comprise an upper protective layer which has an opening for exposing the upper surface (11) of said hydrogen getter layer (10).

4. A device as claimed in claim 1, or as claimed in one of the claims 2 and 3, characterized in that the hydrogen getter layer forms patterns arranged between the integrated circuit elements or patterns arranged along the periphery of the integrated circuits.

5. A device as claimed in one of the claims 1 to 4, characterized in that the semiconductor materials belong to the chemical group III-V.

6. A device as claimed in any one of the claims 1 to 5, characterized in that the material of the hydrogen getter layer comprises palladium (Pd).

7. A device as claimed in any one of the claims 1 to 5, characterized in that the material of the hydrogen getter layer comprises titanium (Ti).

8. A device as claimed in any one of the claims 1 to 7, characterized in that it is enclosed in a housing.

9. A device as claimed in any one of the claims 1 to 8, characterized in that it forms part of a module of a spatial telecommunication system launched in a satellite.

10. A device as claimed in any one of the claims 1 to 8, characterized in that it forms part of a module of a terrestrial telecommunication system.

ABSTRACT:

A semiconductor device comprising integrated circuit elements realized by means of a stack of layers of semiconductor materials provided on a substrate of semiconductor material and comprising means for preventing the pollution of the circuit elements and of the substrate by hydrogen originating from their environment is characterized in that said means are formed by a layer of a material which absorbs hydrogen (or hydrogen getter) (10), which forms a pattern which is integrated with the circuit elements and whose outer surface (11) is exposed and in contact with the environment.

This device, of the MMIC type, forms part of a module of a spatial or terrestrial telecommunication system.

Application: Spatial or terrestrial telecommunication systems.

Reference: Fig. 1A

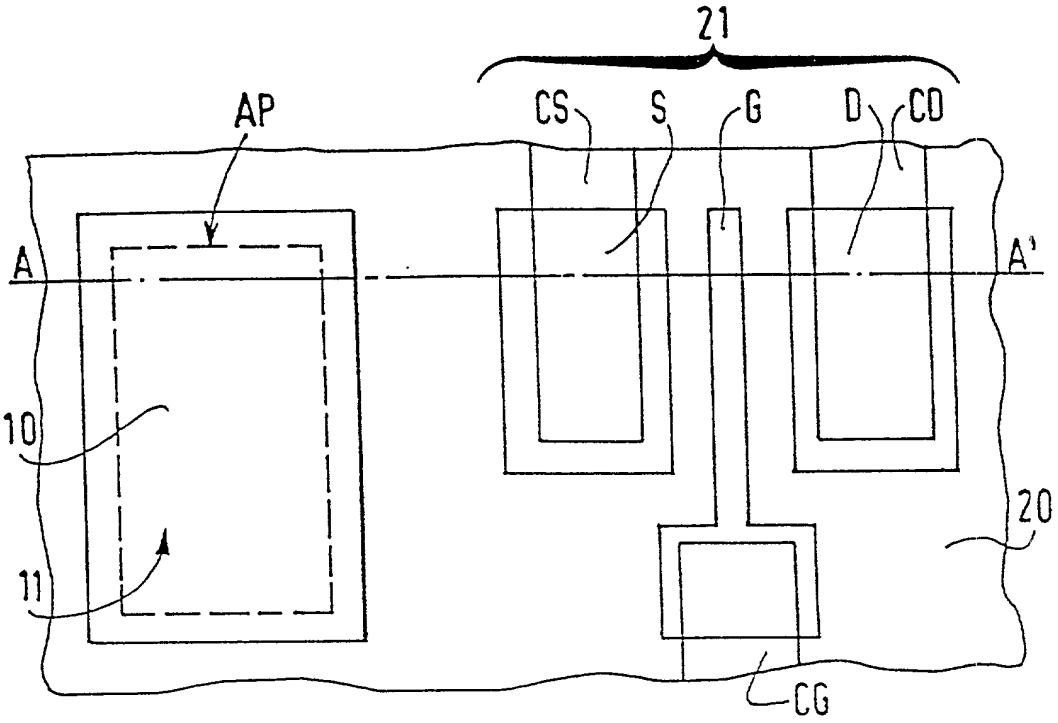
21
AP
CS
S
G
D
CD
A
A'
10
11
20
CG

FIG. 1A

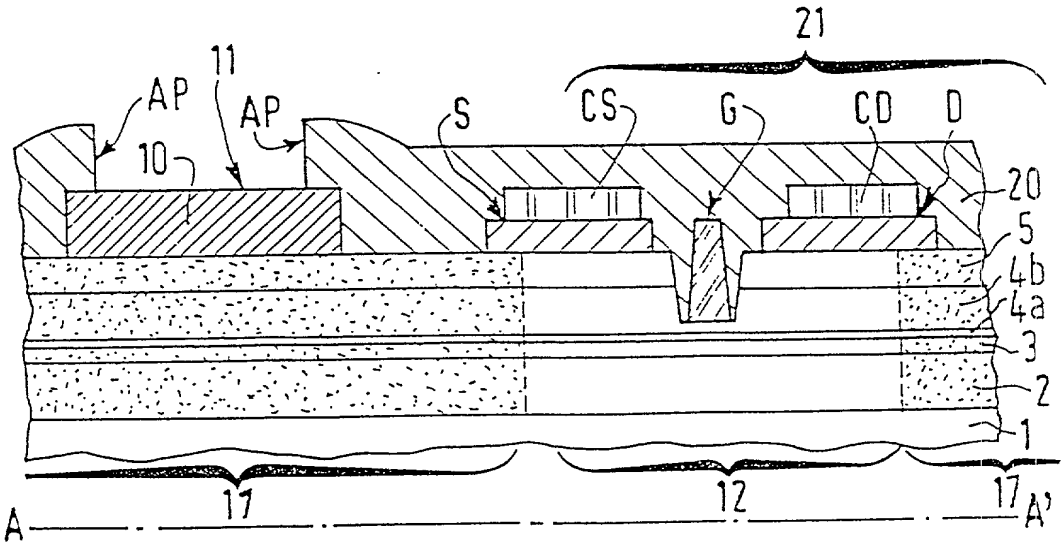
21
11
AP
AP
S
CS
G
CD
D
10
20
5
4b
4a
3
2
1
A
17
12
17
A'

FIG. 1B

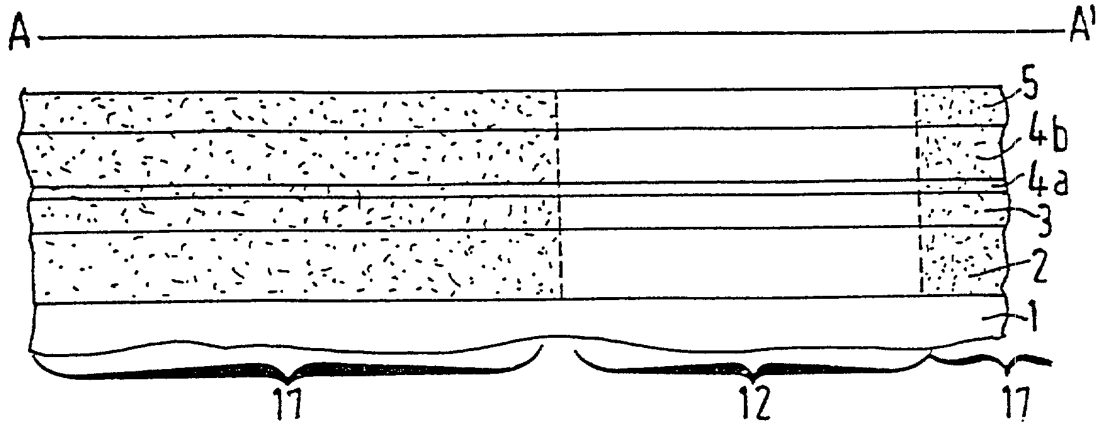

FIG. 2A

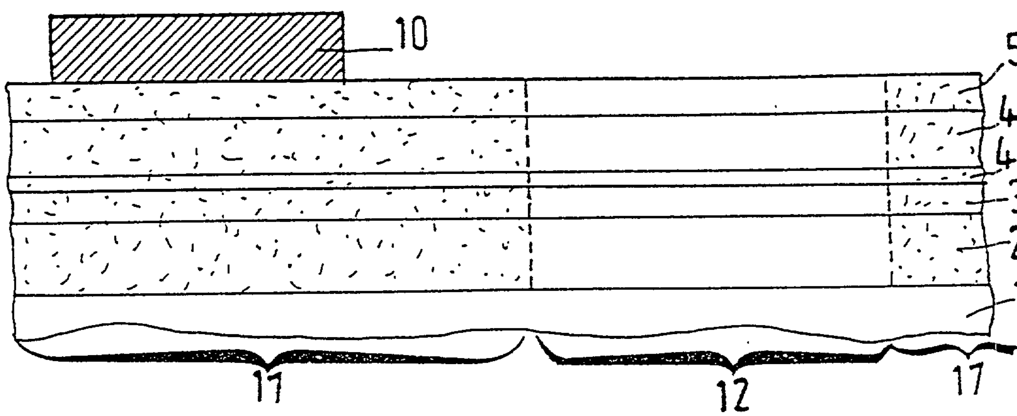

FIG. 2B

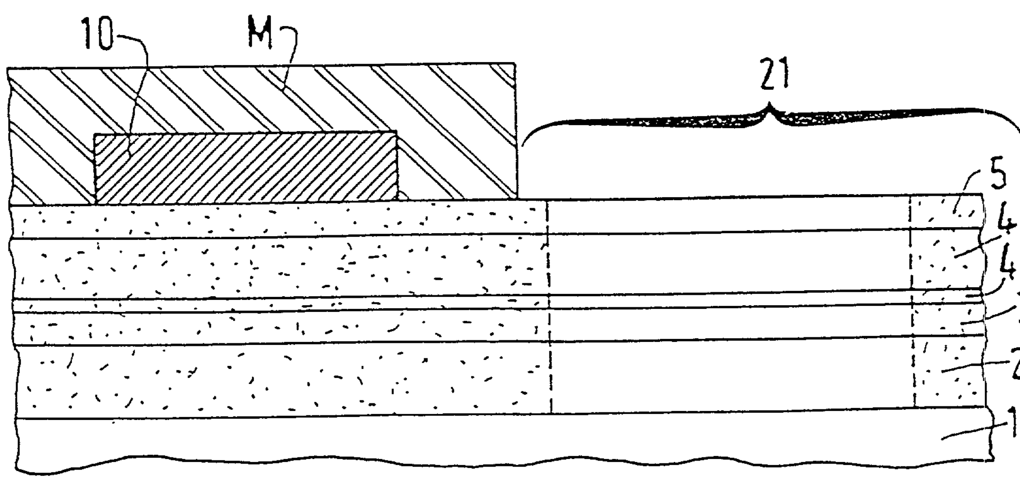

FIG. 2C

DECLARATION and POWER OF ATTORNEY

ATTORNEY'S DOCKET NO.:
PHF 98.601 US

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below next to my name.

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled **"Semiconductor device with integrated circuit elements of group III-V comprising means for preventing pollution by hydrogen"** the specification of which (check one)

☐ is attached hereto.

☐ was filed on _____ as Application Serial No. _____ and was amended on _____ (if applicable).

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claims, as amended by the amendment(s) referred to above.

I acknowledge the duty to disclose information which is material to patentability of this application in accordance with Title 37, Code of Federal Regulations, §1.56(a).

I hereby claim foreign priority benefits under Title 35, United States Code, § 119 of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on which priority is claimed:

PRIOR FOREIGN APPLICATION(S)

COUNTRY	APP. NUMBER	DATE OF FILING (DATE, MONTH, YEAR)	PRIORITY CLAIMED UNDER 35 U.S.C. 119
France	**9812497**	**6 October 1998**	**YES**

I hereby claim the benefit under Title 35, United States Code, §120 of any United States application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35 United States Code, §112, I acknowledge the duty to disclose material information as defined in Title 37, Code of Federal Regulations, §1,56(a) which occurred between the filing date of the prior application and the national or PCT international filing date of this application:

PRIOR UNITED STATES APPLICATION(S)

APPLICATION SERIAL NUMBER	FILING DATE	STATUS (PATENTED, PENDING, ABANDONED)

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

POWER OF ATTORNEY: As a named inventor, I hereby appoint the following attorney(s) and/or agent(s) to prosecute this application and transact all business in the Patent and Trademark Office connected therewith. (list name and registration number)

Algy Tamoshunas, Reg. No. 27,677
Jack E. Haken, Reg. No. 26,902

SEND CORRESPONDENCE TO: Corporate Patent Counsel;	DIRECT TELEPHONE CALLS TO:
U.S. Philips Corporation; 580 white Plains Road;	(name and telephone No.)
Tarrytown, NY 10591	(914) 332-0222

Dated:		Inventor's Signature:		
Full Name of in Inventor	Last Name **BAUDET**	First Name **Pierre**	Middle Name	
Residence & Citizenship	City **Yerres**	State of Foreign Country **France**	Country of Citizenship **France**	
Post Office Address	Street **8 rue Pierre Larousse**	City **91330 Yerres**	State of Country **France**	Zip Code
Dated:		Inventor's Signature:		
Full Name of in Inventor	Last Name **FRIJLINK**	First Name **Peter**	Middle Name	
Residence & Citizenship	City **Yerres**	State of Foreign Country **France**	Country of Citizenship **France**	
Post Office Address	Street **25 rue Frédéric Mistral**	City **91330 Yerres**	State of Country **France**	Zip Code

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of

PIERRE BAUDET ET AL

Atty. Docket

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Honorable Commissioner of Patents and Trademarks
Washington, D.C. 20231

APPOINTMENT OF ASSOCIATES

Sir:

The undersigned Attorney of Record hereby revokes all prior appointments (if any) of Associate Attorney(s) or Agent(s) in the above-captioned case and appoints:

Steven R. Biren (Registration No. 26,531)

c/o U.S. PHILIPS CORPORATION, Intellectual Property Department, 580 White Plains Road, Tarrytown, New York 10591, his Associate Attorney(s)/Agent(s) with all the usual powers to prosecute the above-identified application and any division or continuation thereof, to make alterations and amendments therein, and to transact all business in the Patent and Trademark Office connected therewith.

ALL CORRESPONDENCE CONCERNING THIS APPLICATION AND THE LETTERS PATENT WHEN GRANTED SHOULD BE ADDRESSED TO THE UNDERSIGNED ATTORNEY OF RECORD.

Respectfully,

Jack E. Haken, Reg. 26,902
Attorney of Record

Dated at Tarrytown, New York
this 5TH day of October 1999.

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